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J. White
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Itsuo Hidaka			
Appln. No.: 09/525,802		Art Unit:	2815
Filed: March 15, 2000		Examiner:	L. Cruz
Title: Semiconductor Device		Docket No.	AKM-00301

Certificate of Mailing

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Tracey A. Newell

Tracey A. Newell

AMENDMENT AND RESPONSE

Commissioner for Patents
Washington, D.C. 20231

Sir:

This paper is being provided in response to the Office Action dated January 3, 2002, for the above-captioned U.S. patent application.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required for consideration of this paper (including fees for net addition of claims) are authorized to be charged in two originally-executed copies of an Amendment Transmittal Letter filed herewith.

Attached herewith is a set of "clean" rewritten claims as required by 37 C.F.R. § 1.121.

Kindly enter the following amendments:

IN THE CLAIMS:

Please cancel Claims 10-12 and 18 without prejudice or disclaimer of the subject matter thereof.

Please amend Claims 1, 5, 8, 13 and16 as follows:

1. (Four Times Amended) A semiconductor device having multiple wiring layers, comprising:

a signal line which is formed in a wiring layer, and to which a signal voltage is applied;

two adjacent lines which are so adjacent to said signal line as not to be connected thereto, and which are formed in the same wiring layer where said signal line is formed;

two intersection lines which are respectively formed in wiring layers, each being present via an insulating layer above or under the wiring layer where said signal line and said adjacent lines are formed, and which are formed along a surface area corresponding to an area which is enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through the insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines and said two intersection lines,

wherein said signal line is completely enclosed by said two adjacent lines, said two intersection lines, and said entire-line-area through-holes, which are one of conductors and semiconductors; and

the electric potentials of said two adjacent lines, said two intersection lines, and said entire-line-area through holes have at least one of a plurality of electric potential sources having a selected potential value and a plurality of resistive connections at selected locations to the signal line such that the electric potential has a same phase as a phase of an electric potential of said signal line.

5. (Four Times Amended) A semiconductor device having multiple wiring layers, comprising:

a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;

a plurality of signal lines which are disposed to not intersect each other in a same one wiring layer of said multiple wiring layers, and to which signal voltages having a same phase are applied;

two adjacent lines which are disposed adjacent to both sides of said plurality of signal lines as not to be connected thereto, and which are formed in the wiring layer where said plurality of signal lines are formed;

two intersection lines which are formed in a wiring layer each being present via insulating layers above or under the wiring layer where said plurality of signal lines and said two adjacent lines are formed, and which are formed along, a surface area corresponding to an area enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines with said two intersection lines,

wherein said plurality of signal lines are completely enclosed by said two adjacent lines, said two intersection lines, and said plurality of entire-line-area through-holes, which are one of conductors and semiconductors, and

the electric potentials of said two adjacent lines, said two intersection lines, and said entire-line-area through holes have at least one of a plurality of electric potential sources having a selected potential value and a plurality of resistive connections at selected locations to the signal line such that the electric potential has a same phase as a phase of an electric potential of said signal line.

8. (Four Times Amended) A semiconductor device having multiple wiring layers, said device comprising:

a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;

a plurality of signal lines which are formed not to intersect each other in [an identical] a same wiring layer, and to which signal voltage having different phases are applied;

two first adjacent lines which are so formed adjacent respectively onto a selected outer two of said plurality of signal lines as not to be connected thereto and to be

disposed beyond the edge of the plurality of signal lines, and which are formed in the same wiring layer where said plurality of signal lines are formed;

at least one second adjacent line which is formed in the same wiring layer where said plurality of signal lines are formed, the second adjacent lines being disposed between each individual one of said plurality of signal lines so as not to be connected to said plurality of signal lines;

two intersection lines, each of which is formed in a wiring layer being present via an insulating layer above or under the wiring layer where said signal lines and said first adjacent lines are formed, and each of which is arranged along a surface area corresponding to an area enclosed by said two first adjacent lines; and

entire-line-area through-holes which respectively penetrate through insulating layers formed between said first and second adjacent lines and said two intersection lines along entire areas of said first and second adjacent lines, and which respectively and electrically connect said first and second adjacent lines with said two intersection lines, wherein said plurality of signal lines are completely enclosed by said two first adjacent lines, said at least one second adjacent line, said two intersection lines, and said entire-line-area through-holes, which are one of semiconductors and conductors.

13. (Four Times Amended) A semiconductor device having multiple wiring layers, said device comprising:

a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate having at least five wiring layers;

a first plurality of signal lines which are formed in [different] the second of the wiring layers, and to which signal voltages are respectively applied;

a second plurality of signal lines which are formed in the fourth of the wiring layers, and to which signal voltages are respectively applied;

a plurality of adjacent lines, each pair of which are formed either in [a lowermost or uppermost] the second or fourth wiring layer of the wiring layers where said [plurality of] signal lines are formed, respectively adjacent onto both sides of a selected one of said [plurality of] signal lines which is formed in an identical layer, thereby not to be connected to the selected one of said plurality of signal lines;

two first intersection lines, each of which is formed either in a first wiring layer under the [lowermost] second wiring layer of said first plurality of signal lines, or in a fifth wiring layer above the [uppermost] fourth wiring layer of said second plurality of signal lines, and each of which is formed along a surface area corresponding to an area enclosed by said pair of adjacent lines formed on the both sides of a corresponding one of said [plurality of] signal lines formed either in the [lowermost or uppermost] second or fourth wiring layer of said signal lines;

a second intersection line which is formed in a third wiring layer formed between said wiring layers of said signal lines, and which is formed along a surface area corresponding to at least one area enclosed by said pair of adjacent lines;

a plurality of first entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said first intersection lines, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said two first intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said second intersection line, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said second intersection line,

wherein each said plurality of signal lines are completely enclosed by said plurality of adjacent lines, said two first intersection lines, said second intersection line, said plurality of first entire-line-area through-holes, and said plurality of second entire-line-area through-holes, which are one of conductors and semiconductors, and

wherein the direction of the first plurality of signal lines may be different from the direction of the second plurality of signal lines in any selected area.

16. (Twice Amended) [The semiconductor device according to claim 13,] A semiconductor device having multiple wiring layers, said device comprising:

a plurality of signal lines which are formed in different wiring layers, and to which signal voltages are respectively applied;

a plurality of adjacent lines, each pair of which are formed either in a lowermost or uppermost wiring layer of the wiring layers where said plurality of signal lines are formed, respectively adjacent onto both sides of a selected one of said plurality of signal lines which is formed in an identical layer, thereby not to be connected to the selected one of said plurality of signal lines;

two first intersection lines, each of which is formed either in a wiring layer under the lowermost wiring layer of said signal lines, or in a wiring layer above the uppermost wiring layer of said signal lines, and each of which is formed along a surface area

corresponding to an area enclosed by said pair of adjacent lines formed on the both sides of a corresponding one of said plurality of signal lines formed either in the lowermost or uppermost wiring layer of said signal lines;

a second intersection line which is formed in a wiring layer formed between said wiring layers of said signal lines, and which is formed along a surface area corresponding to at least one area enclosed by said pair of adjacent lines;

a plurality of first entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said first intersection lines, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said two first intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said second intersection line, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said second intersection line,

wherein said plurality of signal lines are completely enclosed by said plurality of adjacent lines, said two first intersection lines, said second intersection line, said plurality of first entire-line-area through-holes, and said plurality of second entire-line-area through-holes, which are one of conductors and semiconductors, and

wherein said signal lines formed in different wiring layers which are adjacent to each other intersect each other.

REMARKS

This paper is being provided in response to the January 3, 2002 Office Action for the above-referenced application. In this response, Applicant has cancelled Claims 10-12 and 18, and amended Claims 1, 5, 8, 13 and 16 in order to more particularly point out and distinctly claim that which Applicant deems to be the claimed invention. Applicant respectfully submits that the modifications to the claims are all supported by the originally filed application.

Applicant thanks the Examiner for the indication of patentable content with regard to Claim 16. In this response, Applicant has amended Claim 16 to be in independent form, and to include the features of base claim 13. Applicant respectfully submits that newly independent Claim 16 is in patentable form, in accordance with the suggestions contained in the Office Action, and requests that Claim 16, as amended herein, be passed to issue.

Nope The objection to the drawing under 37 CFR 1.83(a) as not showing the claimed feature of the plurality of transistors and passive semiconductor devices is hereby traversed and reconsideration thereof is respectfully requested. Applicant believes that the requirement of the law is that drawings may be required when helpful for one of ordinary skill in the art in understanding and interpreting the claimed invention. That the invention clearly includes semiconductor devices may be seen in the title of the invention; at page 1, line 7; page 3, line 26; page 9, line 26; and in general the consistent

use of the term semiconductor device through out the specification. Thus, it is clear that one of ordinary skill in the art would know that there are transistors and other semiconductor devices included in addition to the metal. Applicant believes that since it is clear that there are transistors included in the invention, that the inclusion of transistors and other semiconductor devices in the figures would merely add complexity to the drawing without adding any information or understanding to those of skill in the art.

The rejection of Claims 5-16 and 18 under 35 U.S.C. §112, first paragraph, is hereby traversed and reconsideration thereof is respectfully requested. As noted above with reference to the objection to the drawings, Applicant submits that one of ordinary skill in the art would have no trouble understanding that the invention, entitled a semiconductor device and using well known semiconductor language and techniques throughout the specification, includes and is built above and using standard semiconductor device technology. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

The rejection of Claims 1 and 2 under 35 U.S.C. §102(b) as being anticipated by Cronin et al. (U.S Patent No. 4,776,087, hereinafter referred to as "Cronin") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 1 and 2, as amended herein, are patentably distinct over the cited reference.

Independent Claim 1, as amended, recites a semiconductor device having multiple wiring layers, including a signal line which is formed in a wiring layer, and to which a signal voltage is applied. There are two adjacent lines which are so adjacent to the signal line as not to be connected, and which are formed in the same wiring layer as the signal line is formed. There are two intersection lines which are respectively formed in wiring layers above or under the wiring layer with the signal line and adjacent lines. The intersection lines are formed along a surface area corresponding to an area which is enclosed by the two adjacent lines, forming a box around the signal line. A plurality of entire-line-area through-holes penetrate through the insulating layers formed between the adjacent lines and two intersection lines, along the entire length of the two adjacent lines, and which respectively and electrically connect the two adjacent lines and two intersection lines together. The signal line is thus completely enclosed by the two adjacent lines, the two intersection lines, and the through-holes. The electric potentials of the box made of the adjacent lines, intersection lines, and through holes, have either a plurality of electric potential sources having a selected potential value, or a plurality of resistive connections at selected locations to the signal line such that the electric potential has the same phase as the signal line.

Claim 2 depends from independent Claim 1, and recites further patentable features over the base claim. Dependent claim 2 recites a semiconductor device where the two adjacent lines are substantially parallel to the signal line.

The cited art of Cronin discloses a VLSI coaxial wiring structure having three layers of metal and wherein the outer layer of metal surrounding the signal metal is electrically tied to ground potential (see Cronin's abstract and col. 3, line 63). Along the signal line 56A carrying the high frequency signal, there are two adjacent lines 56, that run along the sides of signal line 56A, and over tungsten plugs 53, that connect to an underlying plate of metal 52, which extends under the signal line 56A from at least each of the two adjacent lines 56. There are overlying tungsten plugs 57, that connect the adjacent lines to a top metal plate that completes the ring around the signal line 56A.

Applicant respectfully submits that the Cronin reference neither discloses nor even suggests ***the electric potentials of said two adjacent lines, said two intersection lines, and said entire-line-area through holes have at least one of a plurality of electric potential sources having a selected potential value and a plurality of resistive connections at selected locations to the signal line such that the electric potential has a same phase as a phase of an electric potential of said signal line***, as set forth in Claim 1. Rather, as pointed out above, Cronin discloses that the lines are electrically connected to the ground plane. Certainly Cronin does not suggest that there may be connections from the signal line to the coaxial conductors.

Amended Claim 1 discloses that the electrical potential of the shield (two adjacent lines, two intersection lines, and entire-line-area through-holes) has the same phase as that of the electric potential of the signal line. That is, the electric potential of the shield cannot generate noise affecting the signal line. On the other hand, the cited reference of

Cronin sets forth the well known limitation that the electric potential of the shield is the ground potential.

Therefore, since the cited reference does not contain each and every feature of the claimed invention, the cited reference can not anticipate independent Claim 1, or Claim 2 which depends therefrom. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

The rejection of Claims 5 - 15 and 18 under 35 U.S.C. §103(a) as being unpatentable over Cronin in view of Ma (U.S. Patent No. 5,729,047, hereinafter referred to as "Ma") is hereby traversed and reconsideration thereof is respectfully requested. Applicant has cancelled Claims 10-12 and 18 and respectfully submits that the rejection as applied to these claims is rendered moot. Applicant respectfully submits that Claims 5 - 9 and 13 -15, as amended herein, are patentably distinct over the cited references, whether taken alone or in any combination.

Independent Claim 5, as amended herein, recites a semiconductor device having multiple wiring layers, including a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate. There is a plurality of signal lines which are disposed to not intersect each other in a same wiring layer, and to which signal voltages having a same phase are applied. There are two adjacent lines which are disposed adjacent to both sides of the signal lines, so as not to be connected, and which are formed in the wiring layer of the signal lines. Two intersection lines are formed in a

wiring layer above or under the wiring layer of the signal lines and adjacent lines, and are formed along a surface area corresponding to an area enclosed by the two adjacent lines. A plurality of entire-line-area through-holes penetrate through insulating layers formed between the adjacent lines and the two intersection lines, along entire areas of the adjacent lines, and which electrically connect the adjacent lines to the intersection lines. The plurality of signal lines are completely enclosed by the adjacent lines, the intersection lines, and entire-line-area through-holes. These lines are made of conductors or semiconductors, and the electric potentials of the adjacent lines, intersection lines, and through holes have either or both of electric potential sources having a selected potential value, or a plurality of resistive connections at selected locations to the signal line such that the electric potential has a same phase as a phase of an electric potential of said signal line. Claims 6 and 7 depend from Claim 5.

Independent Claim 8, as amended herein, recites a semiconductor device having multiple wiring layers, including a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate. A plurality of signal lines are formed to not intersect each other in wiring layer, and signal voltages having different phases are applied. Two first adjacent lines are formed adjacent respectively onto a selected outer two of said plurality of signal lines so as not to be connected, and to be disposed beyond the edge of the plurality of signal lines, and formed in the same wiring layer where the plurality of signal lines are formed. At least one second adjacent line is formed in the same wiring layer as the signal lines are formed, the second adjacent lines being disposed between each individual one of the signal lines so as not to be connected to the signal

lines. Two intersection lines, each of which is formed in a wiring layer being present via an insulating layer above or under the wiring layer of the signal lines and first adjacent lines, and are arranged along a surface area corresponding to an area enclosed by the two first adjacent lines. There are entire-line-area through-holes which respectively penetrate through insulating layers formed between the first and second adjacent lines and the two intersection lines along entire areas of the first and second adjacent lines. The through holes electrically connect the first and second adjacent lines with the two intersection lines. The signal lines are completely enclosed by the two first adjacent lines, the at least one second adjacent line, the two intersection lines, and the entire-line-area through-holes. Claim 9 depends from Claim 8.

Independent Claim 13, as amended herein, recites a semiconductor device having multiple wiring layers, including a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate having at least five wiring layers. There is a first plurality of signal lines which are formed in the second of the wiring layers, and to which signal voltages are respectively applied. There is a second plurality of signal lines which are formed in the fourth of the wiring layers, and to which signal voltages are respectively applied. There is a plurality of adjacent lines, each pair of which are formed either in the second or fourth wiring layer of the wiring layers where said signal lines are formed. Each pair is adjacent to both sides of a selected signal line which is formed in an identical layer, and not connected to the signal lines. There are two first intersection lines, each of which is formed either in a first wiring layer under the second wiring layer of said first plurality of signal lines, or in a fifth wiring layer above

the fourth wiring layer of the signal lines. Each is formed along a surface corresponding to an area enclosed by the pair of adjacent lines. There is a second intersection line which is formed in a third wiring layer between the two wiring layers of signal lines, and formed along a surface corresponding to one area enclosed by the pair of adjacent lines. A plurality of first entire-line-area through-holes penetrate through insulating layers formed between the adjacent lines and first intersection lines, along entire areas of the adjacent lines, thereby electrically connecting the adjacent lines with the two first intersection lines. A plurality of second entire-line-area through-holes penetrate through insulating layers formed between the adjacent lines and the second intersection line, along entire areas of said adjacent lines, thereby electrically connecting the adjacent lines with the second intersection line. Each of the plurality of signal lines are completely enclosed by the adjacent lines, two first intersection lines, second intersection line, the plurality of first entire-line-area through-holes, and the plurality of second entire-line-area through-holes. The direction of the first plurality of signal lines may be different from the direction of the second plurality of signal lines in any selected area. Claims 14-15 depend from Claim 13.

The cited art of Cronin is discussed above. The cited art of Ma discloses a signal isolating and decoupling structure fabricated on an IC. The signal line is embedded in dielectric material (i.e., isolated from other conductor potentials) and enclosed in an isolation structure of conductive material that extends substantially the whole length of the signal conductor (see col. 4, line 67). The system described separates numerous signal lines from outside interference, and protects each signal line from the interference of

other signal lines by having the isolation structure connected to ground, Vss or some other reference voltage (see col. 6, line 61).

Applicant respectfully submits that the cited combination of references, whether taken alone or in any combination, neither discloses nor suggests that ***the electric potentials of said two adjacent lines, said two intersection lines, and said entire-line-area through holes have at least one of a plurality of electric potential sources having a selected potential value and a plurality of resistive connections at selected locations to the signal line such that the electric potential has a same phase as a phase of an electric potential of said signal line***, as set forth in the independent Claim 5, as amended herein. Rather, as discussed above, Cronin sets the shield to ground potential, and Ma sets the shield to some reference voltage, but neither suggests or discloses a problem that might be solved by varying the isolation shield potential in any sort of changing way, let alone in phase with the signal.

Applicant respectfully submits that the cited combination of references, whether taken alone or in any combination, neither discloses nor suggests ***a plurality of signal lines which are formed not to intersect each other in a same wiring layer, and to which signal voltage having different phases are applied; two first adjacent lines which are so formed adjacent respectively onto a selected outer two of said plurality of signal lines as not to be connected thereto and to be disposed beyond the edge of the plurality of signal lines, and which are formed in the same wiring layer where said plurality of signal lines are formed***, as set forth in the independent Claim 8, as amended herein. The

cited reference of Cronin only discloses and suggests single shielded signal wires. The Office Action uses the Ma reference to show that multiple signal wires may be within the shield. However, the Ma reference does not suggest that the adjacent lines that surround the signal wires are made of the same material and at the same time as the signal wires, as recited in the claimed invention. There is no suggestion in the Ma reference that there is any problem with the structure having different metal layers used as the sidewall of the shield, and thus the Office Action is incorrect to suggest that one of skill would obviously see a benefit in the combination, since there is no clear problem to be solved as disclosed in the cited references.

Applicant respectfully submits that the cited combination of references, whether taken alone or in any combination, neither discloses nor suggests that ***the direction of the first plurality of signal lines may be different from the direction of the second plurality of signal lines in any selected area,*** as set forth in the independent Claim 13, as amended herein.

Applicant respectfully submits that neither of the cited references suggest that different layers of signal lines may be running in non parallel directions. The disclosed structures of the cited references can not achieve such an arrangement. The cited reference of Cronin only discloses a single shielded signal line, and thus can not even suggest the possibility of having two layers of signal lines let alone going in different directions. The cited reference of Ma does not use the same metal level as forms the signal lines, for the sidewalls of the shields. Thus the above noted feature is not

suggested in the combination of cited references, and the suggested combination would result in a non operational device since the disclosures are incompatible with respect to the sidewalls of the shield.

The cited combination of references, whether taken alone or in any combination, still neither discloses or suggests at least the above noted features claimed in Applicants' independent Claims, as amended herein, and therefore clearly does not describe or suggest the features of the dependent claims that depend therefrom. Accordingly, Applicant respectfully requests that this rejection, as set forth in the Office Action, be withdrawn.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-951-6676.

Respectfully submitted,
HUTCHINS, WHEELER & DITTMAR

3-18-02
Date

Donald W. Muirhead
Reg. No. 33,978

Patent Group
Hutchins, Wheeler & Dittmar
101 Federal Street
Boston, MA 02110-1804

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1. (Four Times Amended) A semiconductor device having multiple wiring layers, comprising:

a signal line which is formed in a wiring layer, and to which a signal voltage is applied;

two adjacent lines which are so adjacent to said signal line as not to be connected thereto, and which are formed in the same wiring layer where said signal line is formed;

two intersection lines which are respectively formed in wiring layers, each being present via an insulating layer above or under the wiring layer where said signal line and said adjacent lines are formed, and which are formed along a surface area corresponding to an area which is enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through the insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines and said two intersection lines,

wherein said signal line is completely enclosed by said two adjacent lines, said two intersection lines, and said entire-line-area through-holes, which are one of conductors and semiconductors; and

the electric potentials of said two adjacent lines, said two intersection lines, and said entire-line-area through holes have at least one of a plurality of electric potential sources having a selected potential value and a plurality of resistive connections at selected locations to the signal line such that the electric potential has a same phase as a phase of an electric potential of said signal line.

5. (Four Times Amended) A semiconductor device having multiple wiring layers, comprising:

a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;

a plurality of signal lines which are disposed to not intersect each other in a same one wiring layer of said multiple wiring layers, and to which signal voltages having a same phase are applied;

two adjacent lines which are disposed adjacent to both sides of said plurality of signal lines as not to be connected thereto, and which are formed in the wiring layer where said plurality of signal lines are formed;

two intersection lines which are formed in a wiring layer each being present via insulating layers above or under the wiring layer where said plurality of signal lines and said two adjacent lines are formed, and which are formed along, a surface area corresponding to an area enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines with said two intersection lines,

wherein said plurality of signal lines are completely enclosed by said two adjacent lines, said two intersection lines, and said plurality of entire-line-area through-holes, which are one of conductors and semiconductors, and

the electric potentials of said two adjacent lines, said two intersection lines, and said entire-line-area through holes have at least one of a plurality of electric potential

sources having a selected potential value and a plurality of resistive connections at selected locations to the signal line such that the electric potential has a same phase as a phase of an electric potential of said signal line.

8. (Four Times Amended) A semiconductor device having multiple wiring layers, said device comprising:

a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;

a plurality of signal lines which are formed not to intersect each other in a same wiring layer, and to which signal voltage having different phases are applied;

two first adjacent lines which are so formed adjacent respectively onto a selected outer two of said plurality of signal lines as not to be connected thereto and to be disposed beyond the edge of the plurality of signal lines, and which are formed in the same wiring layer where said plurality of signal lines are formed;

at least one second adjacent line which is formed in the same wiring layer where said plurality of signal lines are formed, the second adjacent lines being disposed between each individual one of said plurality of signal lines so as not to be connected to said plurality of signal lines;

two intersection lines, each of which is formed in a wiring layer being present via an insulating layer above or under the wiring layer where said signal lines and said first adjacent lines are formed, and each of which is arranged along a surface area corresponding to an area enclosed by said two first adjacent lines; and

entire-line-area through-holes which respectively penetrate through insulating layers formed between said first and second adjacent lines and said two intersection lines along entire areas of said first and second adjacent lines, and which respectively and electrically connect said first and second adjacent lines with said two intersection lines, wherein said plurality of signal lines are completely enclosed by said two first adjacent

lines, said at least one second adjacent line, said two intersection lines, and said entire-line-area through-holes, which are one of semiconductors and conductors.

13. (Four Times Amended) A semiconductor device having multiple wiring layers, said device comprising:

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a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate having at least five wiring layers;

a first plurality of signal lines which are formed in the second of the wiring layers, and to which signal voltages are respectively applied;

a second plurality of signal lines which are formed in the fourth of the wiring layers, and to which signal voltages are respectively applied;

a plurality of adjacent lines, each pair of which are formed either in the second or fourth wiring layer of the wiring layers where said signal lines are formed, respectively adjacent onto both sides of a selected one of said signal lines which is formed in an identical layer, thereby not to be connected to the selected one of said plurality of signal lines;

two first intersection lines, each of which is formed either in a first wiring layer under the second wiring layer of said first plurality of signal lines, or in a fifth wiring layer above the fourth wiring layer of said second plurality of signal lines, and each of which is formed along a surface area corresponding to an area enclosed by said pair of adjacent lines formed on the both sides of a corresponding one of said signal lines formed either in the second or fourth wiring layer of said signal lines;

a second intersection line which is formed in a third wiring layer formed between said wiring layers of said signal lines, and which is formed along a surface area corresponding to at least one area enclosed by said pair of adjacent lines;

a plurality of first entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said first intersection lines, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said two first intersection lines; and

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a plurality of second entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said second intersection line, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said second intersection line,

wherein each said plurality of signal lines are completely enclosed by said plurality of adjacent lines, said two first intersection lines, said second intersection line, said plurality of first entire-line-area through-holes, and said plurality of second entire-line-area through-holes, which are one of conductors and semiconductors, and

wherein the direction of the first plurality of signal lines may be different from the direction of the second plurality of signal lines in any selected area.

16. (Twice Amended) A semiconductor device having multiple wiring layers, said device comprising:

a plurality of signal lines which are formed in different wiring layers, and to which signal voltages are respectively applied;

a plurality of adjacent lines, each pair of which are formed either in a lowermost or uppermost wiring layer of the wiring layers where said plurality of signal lines are formed, respectively adjacent onto both sides of a selected one of said plurality of signal lines which is formed in an identical layer, thereby not to be connected to the selected one of said plurality of signal lines;

two first intersection lines, each of which is formed either in a wiring layer under the lowermost wiring layer of said signal lines, or in a wiring layer above the uppermost wiring layer of said signal lines, and each of which is formed along a surface area corresponding to an area enclosed by said pair of adjacent lines formed on the both sides of a corresponding one of said plurality of signal lines formed either in the lowermost or uppermost wiring layer of said signal lines;

a second intersection line which is formed in a wiring layer formed between said wiring layers of said signal lines, and which is formed along a surface area corresponding to at least one area enclosed by said pair of adjacent lines;

a plurality of first entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said first intersection lines, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said two first intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said second intersection line, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said second intersection line,

wherein said plurality of signal lines are completely enclosed by said plurality of adjacent lines, said two first intersection lines, said second intersection line, said plurality of first entire-line-area through-holes, and said plurality of second entire-line-area through-holes, which are one of conductors and semiconductors, and

wherein said signal lines formed in different wiring layers which are adjacent to each other intersect each other.